

Fig. 1

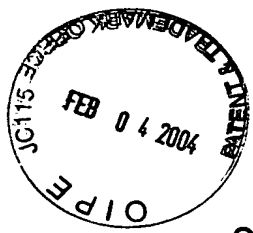
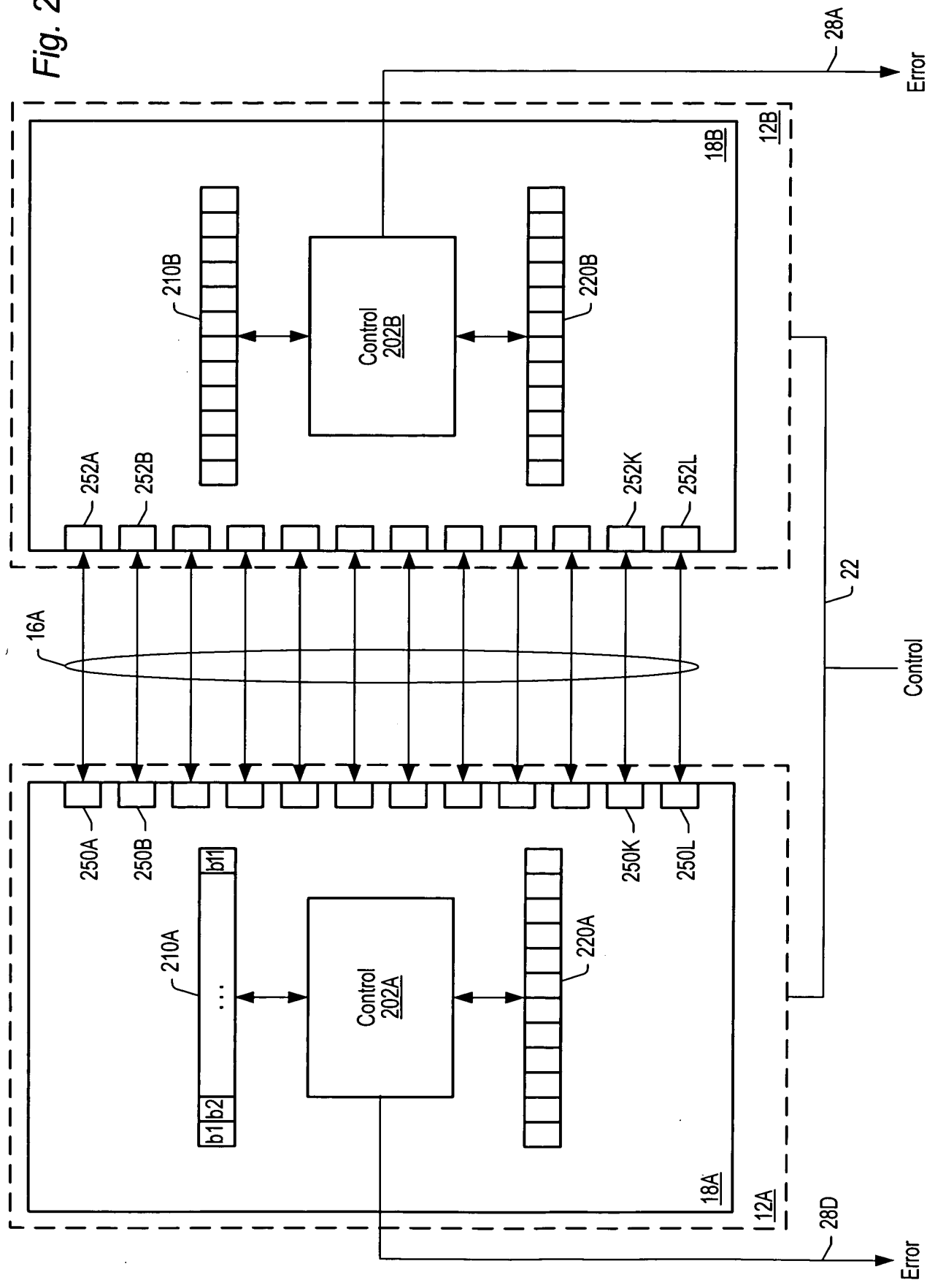


Fig. 2

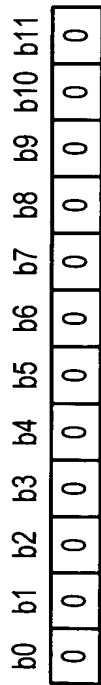


16 cycle pattern driving sequence.



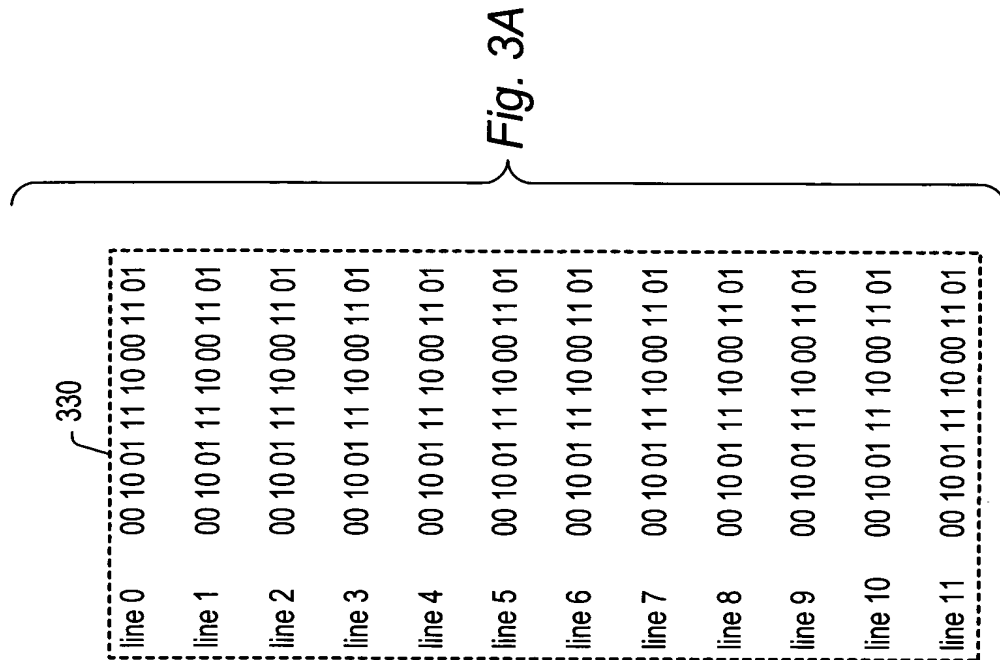
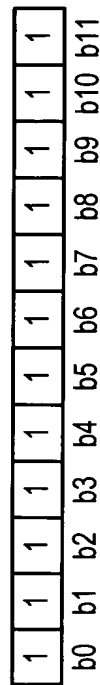
Pattern 1

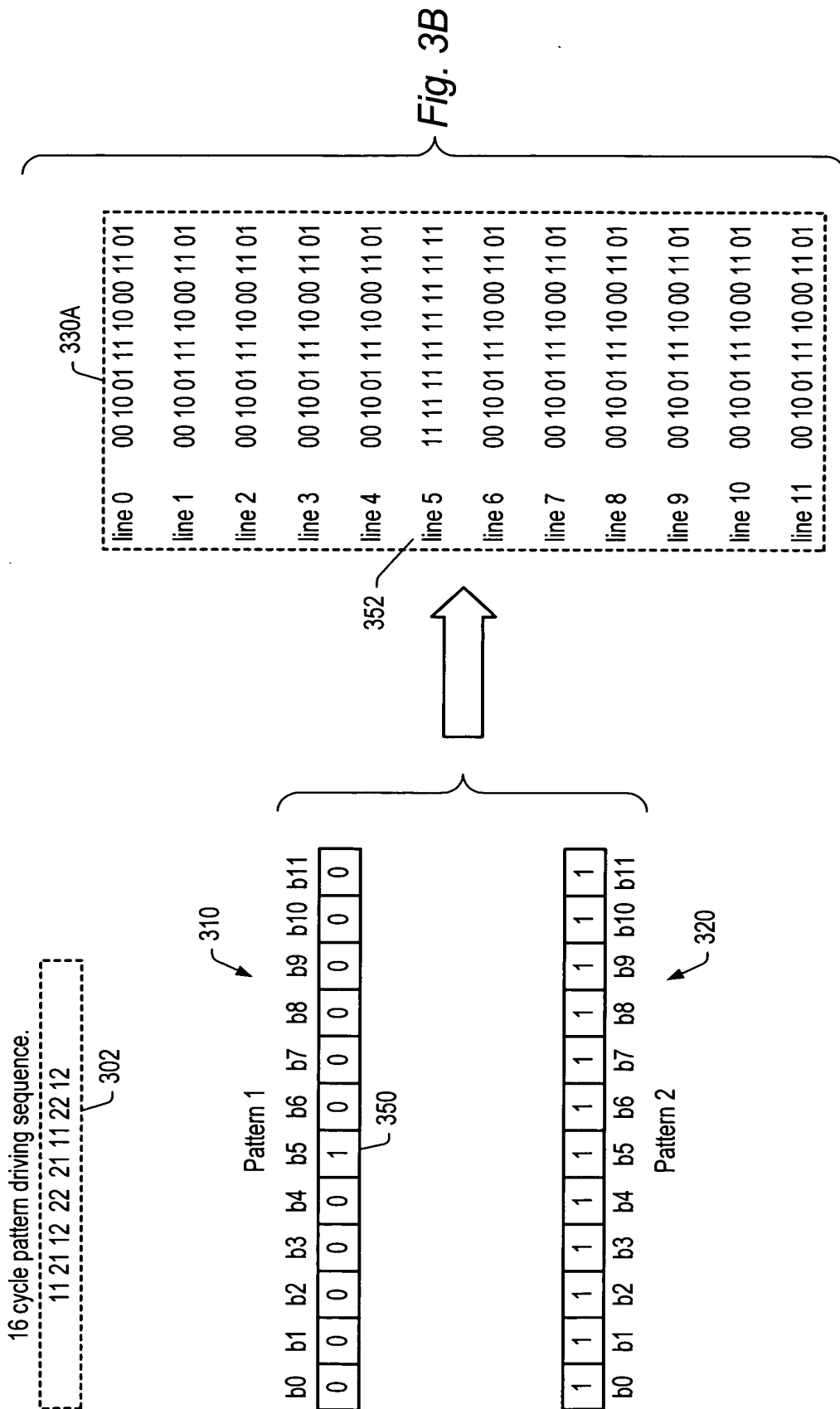
310

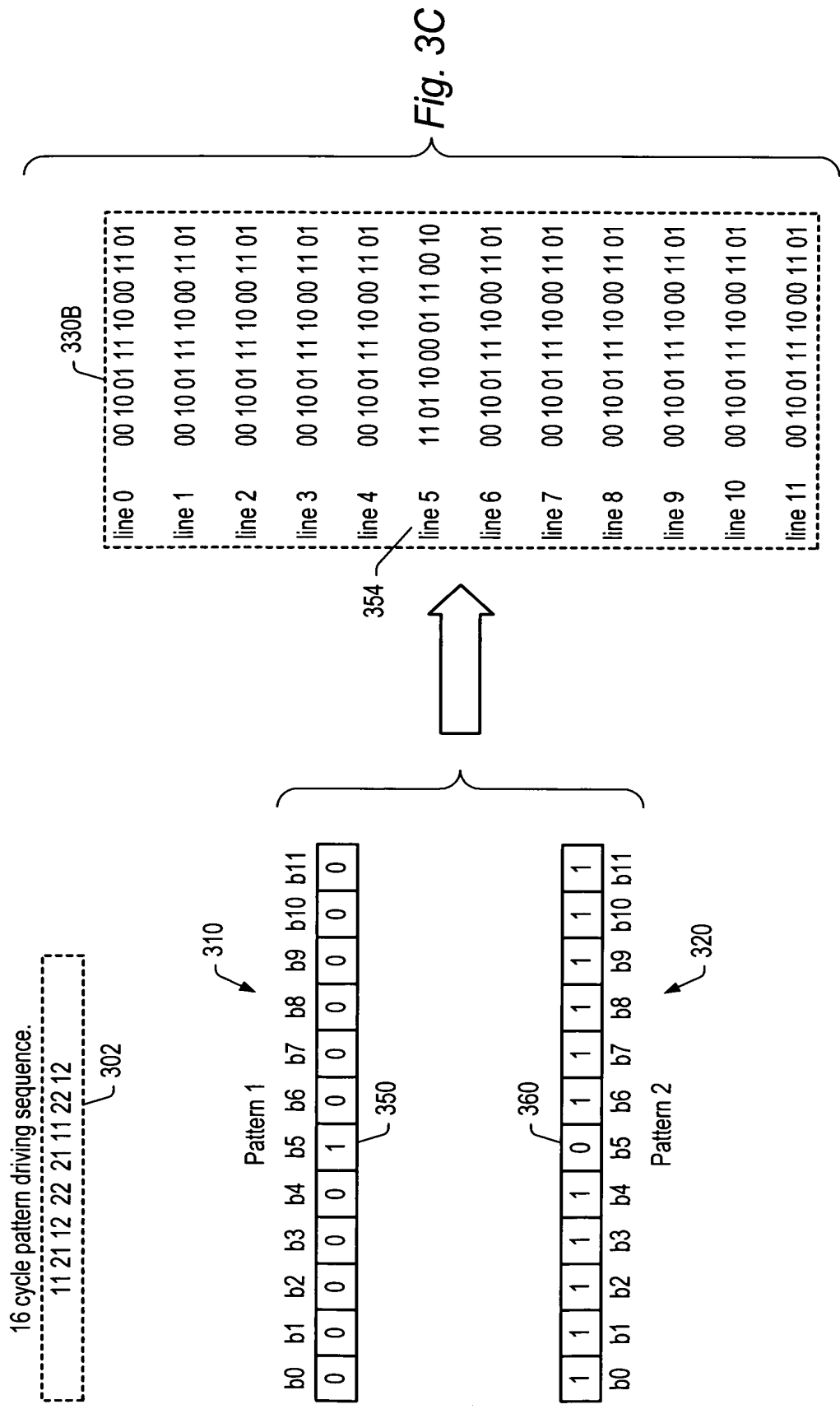


Pattern 2

320







6 / 9

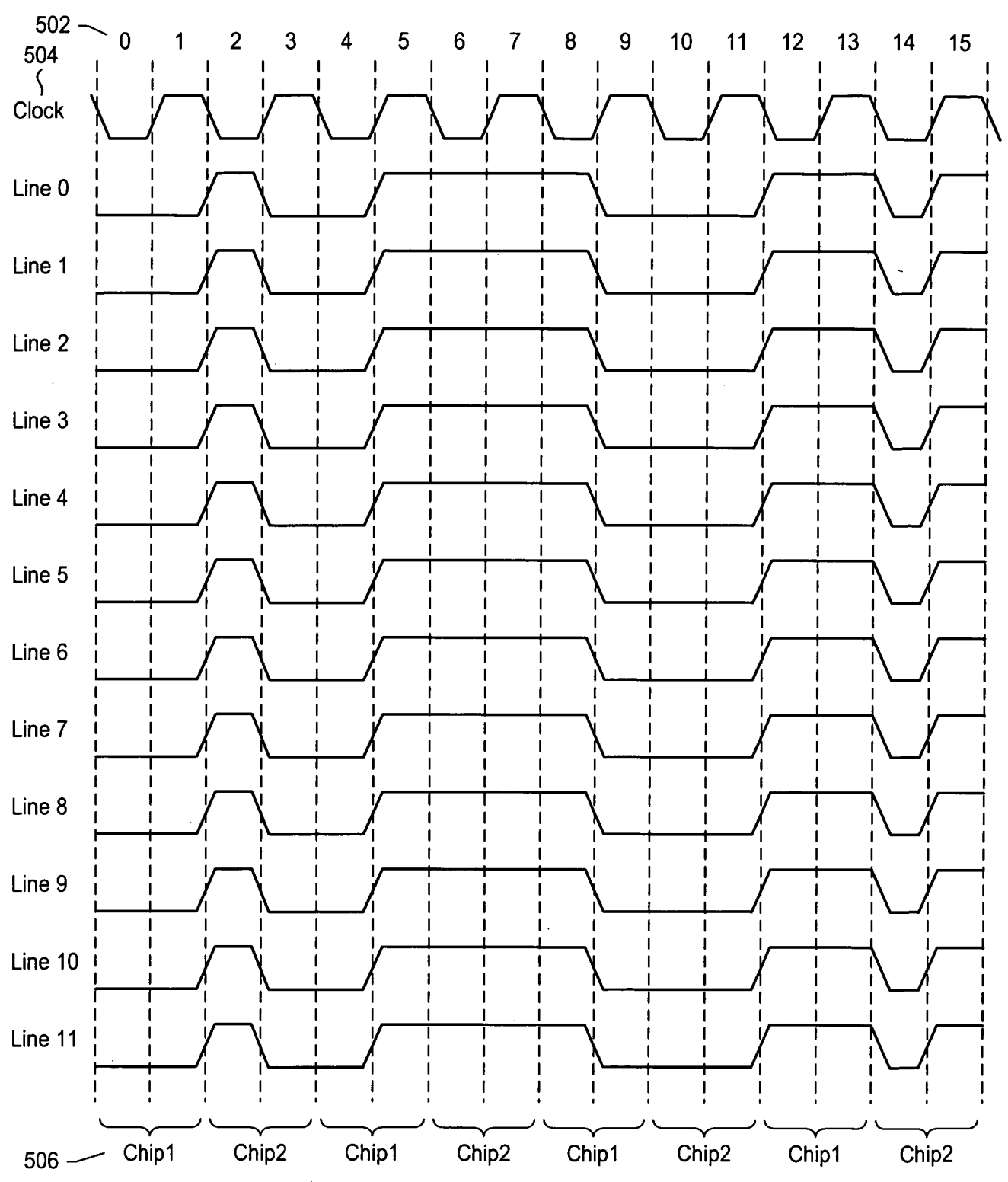
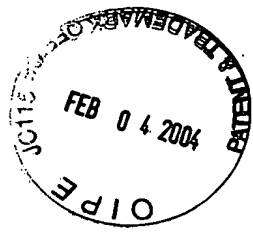


Fig. 5

The timing diagram illustrates the relationship between a clock signal, data bus, and address bus over 60 clock cycles. The clock signal (602) is a periodic square wave. The data bus (604) consists of 12 bits (Bit 0 to Bit 11). The address bus (606) consists of 12 bits (Chip 1 to Chip 12). The diagram shows that the data bus is active during the first 12 clock cycles, and the address bus is active during the next 12 clock cycles. The data bus is then active again during the next 12 clock cycles, and the address bus is active during the final 12 clock cycles. The data bus is active during the first 12 clock cycles, and the address bus is active during the next 12 clock cycles. The data bus is then active again during the next 12 clock cycles, and the address bus is active during the final 12 clock cycles.



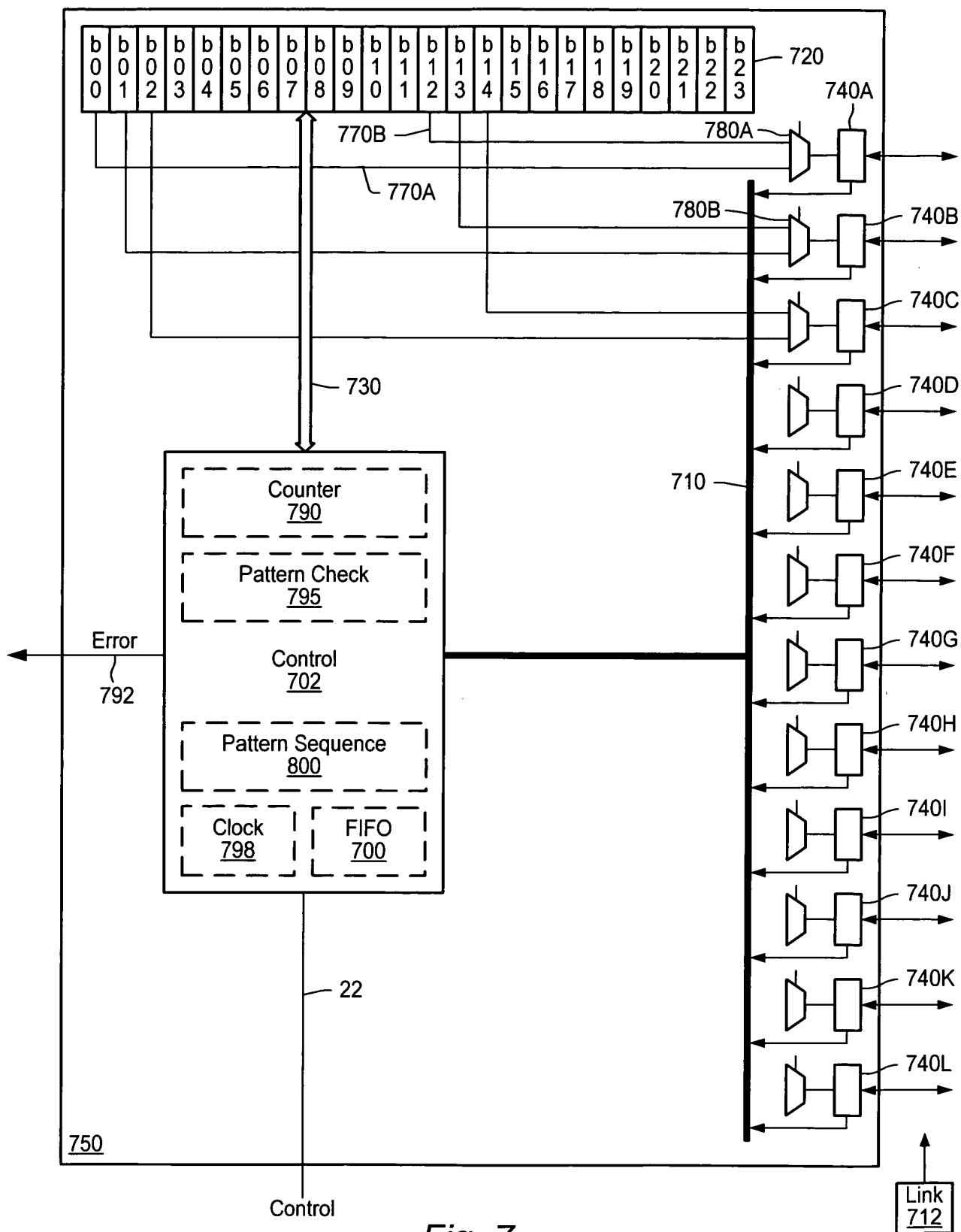


Fig. 7